

Register Test Plan

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1. VeriChip in: **RESET** state (section 6.1)

1.1 Objective

- a. Verify Registers Return to default values after reset.
- b. Make sure Version and Result Output registers are read only.
- c. Validate reserved bits remain unchanged
- d. Ensure that byte_en has no effect.

1.2 Test Plan:

Test Name	Register	Read (R)/ Write (W)	Specification Reference	Address	Test Description Write the following values	Expected Result Read the values after each write (after Reset triggered)
Reg_version_reset	Version	R	5.1	0x00	After reset, read the version register.	16'h0210 if (export_disable==0) or 16'h8210 if (export_disable==1)
Reg_status_reset	Status	R&W	5.2	0x04	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0000 iii. 16'h0000 iv. 16'h0000
Reg_command_reset	Command	R&W	5.3	0x08	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0000 iii. 16'h0000 iv. 16'h0000
Reg_configuration_reset	Configuration	R&W	5.4	0x0C	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0000 iii. 16'h0000 iv. 16'h0000
Reg_left_alu_reset	Left ALU Input	R&W	5.5	0x10	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0000 iii. 16'h0000 iv. 16'h0000
Reg_right_alu_reset	Right ALU Input	R&W	5.6	0x14	i. 16'h0000 ii. 16'h5555	i. 16'h0000 ii. 16'h0000 iii. 16'h0000

					iii. 16'hAAAA iv. 16'hFFFF	iv. 16'h0000
Reg_result_reset	Result Output	R	5.7	0x18	After reset, read the Result register.	16'h0000

1.3 Footnote:

- a. All registers should reset to their default values as per the specification.
- b. Ensure chip_select is enabled while doing any operation.
- c. Write should have no effect during the reset state.
- d. Read should return the default reset values.
- e. Ensure there is no aliasing or cross register interference.
- f. Reserved bits should never change and should always remain 0:
 - a. 14:12 for version register,
 - b. 7:4 for status register,
 - c. 14:4 for command register,
 - d. 7:0 for configuration register

2. VeriChip in: **NORMAL** state (Section 6.2)

2.1 Objective:

- a. Ensure interrupts function as expected.
- b. Make sure reserved bits remain unchanged.
- c. Confirm registers can be successfully read/written during normal operations.

2.2 Test Plan:

Test Name	Register	Read (R)/ Write (W)	Specification Reference	Address	Test Description	Expected Result
Reg_version_normal	Version	R	5.1	0x00	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	Read the values after each write 16'h0210 if (export_disable==0) or 16'h8210 if (export_disable==1)

Reg_status_normal	Status	R&W	5.2	0x04	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0100 iii. 16'h0200 iv. 16'h0300
Reg_command_normal	Command	R&W	5.3	0x08	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0005 iii. 16'h000A iv. 16'h000F
Reg_configuration_normal	Configuration	R&W	5.4	0x0C	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h0100 iii. 16'h0200 iv. 16'h0300
Reg_left_alu_normal	Left ALU Input	R&W	5.5	0x10	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF
Reg_right_alu_normal	Right ALU Input	R&W	5.6	0x14	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF
Reg_result_normal	Result Output	R	5.7	0x18	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF	i. 16'h0000 ii. 16'h5555 iii. 16'hAAAA iv. 16'hFFFF

2.3 Footnote:

- a. Read and write operations should function based on access permissions.
- b. Testing the result output register, writing the values mean specifying values in ALU left ,Right registers and Command register to get the desired input to test if the value is getting read (Eg: ALU left has 16'h5555 ALU right has 16'h0000 using addition operation of ALU we could get 16'h5555 in the result register).
- c. Registers should retain their values unless explicitly modified.
- d. Ensure chip_select is enabled while doing any operation.
- e. Special function registers (e.g., ALU Output, Status) should reflect correct values based on operational inputs.
- f. Reserved bits should never change and should always remain 0:
 - a. 14:12 for version register,
 - b. 7:4 for status register,
 - c. 14:4 for command register,
 - d. 7:0 for configuration register

2.4 Byte Enable test cases

2.4.1 2'b00: No writes, Register remains unchanged.

2.4.2 2'b01: Lower Bytes only, updates only the LSB

2.4.3 2'b10: Upper Bytes only, updates only the MSB

2.4.4 2'b11: Overwrites the register.

Write Data	Byte_en	Register Value (Initially)	Expected Result
i. 16'h0000 ii. 16'h0000 iii. 16'h0000	i. 2'b01 ii. 2'b10 iii. 2'b11	i. 16'h5555 ii. 16'h5555 iii. 16'h5555	i. 16'h5500 ii. 16'h0055 iii. 16'h0000
i. 16'h5555 ii. 16'h5555 iii. 16'h5555	i. 2'b01 ii. 2'b10 iii. 2'b11	i. 16'h1111 ii. 16'h1111 iii. 16'h1111	i. 16'h1155 ii. 16'h5511 iii. 16'h5555
i. 16'hAAAA ii. 16'hAAAA iii. 16'hAAAA	i. 2'b01 ii. 2'b10 iii. 2'b11	i. 16'h0000 ii. 16'h0000 iii. 16'h0000	i. 16'h00AA ii. 16'hAA00 iii. 16'hAAAA
i. 16'hFFFF ii. 16'hFFFF iii. 16'hFFFF	i. 2'b01 ii. 2'b10 iii. 2'b11	i. 16'h8888 ii. 16'h8888 iii. 16'h8888	i. 16'h88FF ii. 16'hFF88 iii. 16'hFFFF

2.5 Aliasing test

Aliasing occurs when two or more addresses point to the same memory location, causing anomalies.

Sample Aliasing **test Plan** for Left ALU Input and Version registers:

Test Step	Register	Address	Operation	Write Data	Expected Outcome
1.	Left ALU Input	0x10	Write	0xAAAA	Writes to the ALU left register
2.	Left ALU Input Aliased	0x50	Read	No Write	0xAAAA
3.	Left ALU Input Aliased	0x50	Write	0x5555	Writes to the ALU left register

4.	Left ALU Input	0x10	Read	No Write	0x5555
5.	Version Register	0x00	Read	No Write	16'h0210 if (export_disable==0) or 16'h8210 if (export_disable==1)
6.	Version Register Aliased	0x40	Read	No Write	16'h0210 if (export_disable==0) or 16'h8210 if (export_disable==1)

3. VeriChip in: **Export Violation** state (Section 6.3)

3.1 Objective

- a. Make sure Read and Write return default/predefined error value.
- b. Validate Register access is restricted.
- c. Verify that reserved bits remain unaffected.

3.2 Test Plan:

Test Name	Register	Read (R)/ Write (W)	Specification Reference	Address	Test Description	Expected Result
Reg_version_export_violation	Version	R	5.1	0x00	Attempt to read in export violation state	16'h0000
Reg_status_export_violation	Status	R&W	5.2	0x04	Attempt to read & write in export violation state	16'h0208 (No matter what is written)
Reg_command_export_violation	Command	R&W	5.3	0x08	Attempt to read & write in export violation state	16'h0000
Reg_configuration_export_violation	Configuration	R&W	5.4	0x0C	Attempt to read & write in export violation state	16'h0000

Reg_left_alu_export_violation	Left ALU Input	R&W	5.5	0x10	Attempt to read & write in export violation state	16'h0000
Reg_right_alu_export_violation	Right ALU Input	R&W	5.6	0x14	Attempt to read & write in export violation state	16'h0000
Reg_result_export_violation	Result Output	R	5.7	0x18	Attempt to read in export violation state	16'h0000

3.3 Footnote:

- a. Registers that store critical data should not expose information.
- b. Ensure chip_select is enabled while doing any operation.
- c. If the read-back for bit 15 is 1, the register will have failed the test because the version register is a read-only register, and that bit follows the export disable input control signal.
- d. Ensure that commands meant to modify system state do not execute in this mode.
- e. Reserved bits should never change and should always remain 0:
 - a. 14:12 for version register,
 - b. 7:4 for status register,
 - c. 14:4 for command register,
 - d. 7:0 for configuration register

4. VeriChip in: **Error** state (Section **6.4**)

4.1 Objective

- a. Verify all registers behave correctly in this state.
- b. Ensure read only registers retain their value.

4.2 Test Plan

Test Name	Register	Read (R)/ Write (W)	Specification Reference	Address	Test Description	Expected Result
Reg_version_error	Version	R	5.1	0x00	Attempt to read in error state	16'h0210 if (export_disable==0) or 16'h8210 if (export_disable==1)
Reg_status_error	Status	R&W	5.2	0x04	Attempt to read & write in error state	16'h0000 (Read only, Write disabled)
Reg_command_error	Command	R&W	5.3	0x08	Attempt to read & write in error state	16'h0000 (Read only, Write disabled)
Reg_configuration_error	Configuration	R&W	5.4	0x0C	Attempt to read & write in error state	16'h0000 (Read only, Write disabled)
Reg_left_alu_error	Left ALU Input	R&W	5.5	0x10	Attempt to read & write in error state	16'h0000 (Read only, Write disabled)
Reg_right_alu_error	Right ALU Input	R&W	5.6	0x14	Attempt to read & write in error state	16'h0000 (Read only, Write disabled)
Reg_result_error	Result Output	R	5.7	0x18	Attempt to read in error state	Retains previous Value.

4.3 Footnote:

- a. Write operations should be disabled/ restricted.
- b. Ensure chip_select is enabled while doing any operation.
- c. Status and error indicators should correctly reflect fault conditions.
- d. Alias testing should confirm that error state protections extend across all mapped register addresses.

- e. Reserved bits should never change and should always remain 0:
 - a. 14:12 for version register,
 - b. 7:4 for status register,
 - c. 14:4 for command register,
 - d. 7:0 for configuration register
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Thank You